Claims

[c1] 1. A flip-chip die having an active surface with a plurality of core power/ground pads, at least one signal pad ring, at least one power pad ring and at least one ground pad ring thereon, wherein the core power/ground pads are located in the central region of the die while the signal pad ring, the power pad ring and the ground pad ring are located outside the central power/ground pad region but concentric to the central power/ground pad region.

[c2] 2. The flip-chip die of claim 1, wherein the signal pad ring encloses a plurality of die pads such that over 50% of the die pads within the signal pad ring is signal pads.

[c3] 3. The flip-chip die of claim 1, wherein the signal pad ring encloses a plurality of die pads and the die pads are positioned as a multiple of rings.

[c4] 4. The flip-chip die of claim 1, wherein the power pad ring includes a plurality of die pads such that over 50% of the die pads within the power pad ring is power pads.

[c5] 5. The flip-chip die of claim 1, wherein the power pad ring encloses a plurality of die pads and the die pads are positioned as a multiple of rings.

[c6] 6. The flip-chip die of claim 1, wherein the ground pad ring includes a plurality of die pads such that over 50% of the die pads within the ground pad ring is ground pads.

[c7] 7. The flip-chip die of claim 1, wherein the ground pad ring encloses a plurality of die pads and the die pads are positioned as a multiple of rings.

[c8] 8. A flip-chip package substrate, comprising:
a plurality of wiring layers forming a stack;
a plurality of insulation layers sandwiched between two neighboring wiring layers for isolating the wiring layers such that an insulation layer and a wiring layer stack on top of each other alternately; and
a plurality of conductive plugs passing through the insulation layer for connecting the wiring layers electrically;

wherein the uppermost layer of the wiring layers has a plurality of core power/ground bump pads, at least one signal bump pad rings, at least one power bump pad rings and at least one ground bump pad rings, the core power/ground pads are located in the central region of the package substrate while the signal pad ring, the power pad ring and the ground pad ring are located outside the central power/ground pad region but concentric to the central power/ground pad region.

[c9] 9. The flip-chip package substrate of claim 8, wherein the signal bump pad ring encloses a plurality of bump pads such that over 50% of the bump pads within the signal bump pad ring is signal bump pads.

[c10] 10. The flip-chip package substrate of claim 8, wherein the signal bump pad ring encloses a plurality of bump pads and the bump pads are positioned as a multiple of rings.

[c11] 11. The flip-chip package substrate of claim 8, wherein the power bump pad ring includes a plurality of bump pads such that over 50% of the bump pads within the power bump pad ring is power bump pads.

[c12] 12. The flip-chip package substrate of claim 8, wherein the power bump pad ring encloses a plurality of bump pads and the bump pads are positioned as a multiple of rings.

[c13] 13. The flip-chip package substrate of claim 8, wherein the ground bump pad ring includes a plurality of bump pads such that over 50% of the bump pads within the ground bump pad ring is ground bump pads.

[c14] 14. The flip-chip package substrate of claim 8, wherein the ground bump pad ring encloses a plurality of bump pads and the bump pads are positioned as a multiple of rings.

[c15]

15. A flip-chip package substrate, comprising:
a plurality of wiring layers forming a stack;
a plurality of insulation layers sandwiched between two neighboring wiring layers for isolating the wiring layers such that an insulation layer and a wiring

layer stack on top of each other alternately; and

a plurality of conductive plugs passing through the insulation layer for connecting the wiring layers electrically;

wherein the uppermost layer of the wiring layers has a plurality of core power/ground bump pads, at least one signal bump pad rings, at least one power bump pad rings and at least one ground bump pad rings, the core power/ground pads are located in the central region of the die while the signal pad ring, the power pad ring and the ground pad ring are located outside the central power/ground pad region but concentric to the central power/ground pad region;

wherein at least one non-signal bump pad ring encloses at least one signal bump pad ring; and

wherein at least one wiring layer has at least one signal trace, and at least one guard traces and the guard trace is adjacent to the signal trace.

[c16] 16. The flip-chip package substrate of claim 15, wherein the signal bump pad ring encloses a plurality of bump pads such that over 50% of the bump pads within the signal bump pad ring is signal bump pads.

[c17] 17. The flip-chip package substrate of claim 15, wherein the signal bump pad ring encloses a plurality of bump pads and the bump pads are positioned as a multiple of rings.

[c18] 18. The flip-chip package substrate of claim 15, wherein the power bump pad ring includes a plurality of bump pads such that over 50% of the bump pads within the power bump pad ring is power bump pads.

[c19] 19. The flip-chip package substrate of claim 15, wherein the power bump pad ring encloses a plurality of bump pads and the bump pads are positioned as a multiple of rings.

[c20] 20. The flip-chip package substrate of claim 15, wherein the ground bump pad ring includes a plurality of bump pads such that over 50% of the bump pads within the ground bump pad ring is ground bump pads.

[c21] 21. The flip-chip package substrate of claim 15, wherein the ground bump pad

ring encloses a plurality of bump pads and the bump pads are positioned as a multiple of rings.

[c22] 22. The flip-chip package substrate of claim 15, wherein the guard trace is a power trace.

[c23] 23. The flip-chip package substrate of claim 15, wherein the guard trace is a ground trace.

[c24] 24. The flip-chip package substrate of claim 15, wherein the non-signal bump pad ring is a power bump pad ring.

[c25] 25. The flip-chip package substrate of claim 15, wherein the non-signal bump pad ring is a ground bump pad ring.